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Inventor Name Search Result

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Last Name = LEE
First Name = SANG-HYUN

Application#	Patent#	Status	Date Filed	Title	Inventor Name 38
60622698	Not Issued	020	10/28/2004	METHOD FOR READING BCA CODE WITHOUT FG (FREQUENCY GENERATOR)	LEE, SANG-HYUN
60590710	Not Issued	020	07/22/2004	DIVIDE-BY-16.5 FREQUENCY DIVIDER WITH CASCADED DIVIDE-BY-3 AND DIVIDE-BY-5.5 DIVIDERS AND DEVICES INCLUDING SAME	LEE, SANG-HYUN
60416017	Not Issued	159	10/04/2002	2.5-10GBPS CMOS TRANSCEIVER WITH ALTERNATING EDGE SAMPLING PHASE DETECTION FOR LOOP CHARACTERISTIC STABILIZATION	LEE, SANG-HYUN
60229369	Not Issued	159	08/30/2000	DATA RECOVERY USING DATA EYE TRACKING	LEE, SANG-HYUN
29122719	D442175	150	05/03/2000	CASE FOR A PERSONAL COMPUTER	LEE, SANG-HYUN
11107846	Not Issued	020	04/18/2005	FIELD EMISSION DEVICE (FED)	LEE, SANG-HYUN
11105922	Not Issued	030	04/13/2005	DECODING APPARATUS FOR LOW-DENSITY PARITY-CHECK CODES USING SEQUENTIAL DECODING, AND METHOD THEREOF	LEE, SANG-HYUN
11073246	Not Issued	030	03/04/2005	TRANSISTORS OF SEMICONDUCTOR DEVICE HAVING CHANNEL REGION IN A CHANNEL-PORTION HOLE AND METHODS OF FORMING THE SAME	LEE, SANG-HYUN
11066854	Not Issued	020	02/24/2005	METHOD FOR FORMING ELECTRON EMISSION SOURCE FOR ELECTRON EMISSION DEVICE AND ELECTRON EMISSION DEVICE USING THE SAME	LEE, SANG-HYUN
11056995	Not Issued	019	02/11/2005	PHASE LOCK LOOP WITH COARSE CONTROL LOOP	LEE, SANG-HYUN

				HAVING FREQUENCY LOCK DETECTOR AND DEVICE INCLUDING SAME	
11051834	Not Issued	020	02/04/2005	RECESSED-TYPE FIELD EFFECT TRANSISTOR WITH REDUCED BODY EFFECT	LEE, SANG-HYUN
11048809	Not Issued	030	02/03/2005	METHOD OF MANUFACTURING FIELD EMITTER	LEE, SANG-HYUN
11022056	Not Issued	019	12/23/2004	RECESS TYPE MOS TRANSISTOR AND METHOD OF MANUFACTURING SAME	LEE, SANG-HYUN
11021349	Not Issued	030	12/23/2004	ASYMMETRIC MOS TRANSISTOR WITH TRENCH-TYPE GATE	LEE, SANG-HYUN
11000290	Not Issued	020	11/29/2004	APPARATUS AND METHOD FOR ERASURE DETECTION AND SOFT-DECISION DECODING IN CELLULAR SYSTEM RECEIVER	LEE, SANG-HYUN
10964122	Not Issued	020	10/12/2004	APPARATUS FOR ENCODING AND DECODING OF LOW-DENSITY PARITY-CHECK CODES, AND METHOD THEREOF	LEE, SANG-HYUN
10912055	Not Issued	020	08/06/2004	LASER DIODE DRIVING CIRCUIT AND LASER DIODE CONTROLLING APPARATUS INCLUDING THE LASER DIODE DRIVING CIRCUIT	LEE, SANG-HYUN
10896169	Not Issued	020	07/22/2004	GENE ENCODING CYSTEINE PROTEASE AND ITS PROMOTER WHICH ARE EXPRESSED SPECIFICALLY IN RICE ANTHER, A METHOD FOR PRODUCING MALE STERILE RICE BY SUPPRESSING EXPRESSION OF THE GENE	LEE, SANG-HYUN
10845393	Not Issued	030	05/12/2004	COVER REPLACEMENT ASSEMBLY FOR A MOBILE COMMUNICATION TERMINAL	LEE, SANG-HYUN
10740573	Not Issued	030	12/22/2003	MONOLITHIC INK-JET PRINTHEAD AND METHOD FOR MANUFACTURING THE SAME	LEE, SANG-HYUN
10723528	Not Issued	030	11/25/2003	ADAPTIVE TRANSMISSION AND RECEIVING METHOD AND DEVICE IN WIRELESS COMMUNICATION SYSTEM WITH MULTIPLE ANTENNAS	LEE, SANG-HYUN
10696897	Not Issued	030	10/29/2003	SIMPLIFIED MESSAGE-PASSING DECODER FOR LOW-DENSITY PARITY-CHECK CODES	LEE, SANG-HYUN
10688079	6838341	150	10/16/2003	METHOD FOR FABRICATING	LEE, SANG-HYUN

				SEMICONDUCTOR DEVICE WITH SELF-ALIGNED STORAGE NODE	
10665085	Not Issued	020	09/17/2003	HYBRID MULTI-USER INTERFERENCE CANCELLATION METHOD AND DEVICE USING CLUSTERING ALGORITHM BASED ON DYNAMIC PROGRAMMING	LEE, SANG-HYUN
10642259	Not Issued	030	08/15/2003	DATA SAMPLING METHOD AND APPARATUS WITH ALTERNATING EDGE SAMPLING PHASE DETECTION FOR LOOP CHARACTERISTIC STABILIZATION	LEE, SANG-HYUN
10606822	Not Issued	020	06/26/2003	DIGITAL FILTER FOR SOFTWARE-DEFINED RADIO SYSTEM, DIGITAL INTERMEDIATE FREQUENCY SIGNAL PROCESSING APPARATUS HAVING THE DIGITAL FILTER, AND METHOD THEREOF	LEE, SANG-HYUN
10334352	Not Issued	040	12/31/2002	METHOD AND DEVICE FOR PERFORMING SOFT DECISION DECODING ON REED-MULLER CODES USING DECISION BY MAJORITY	LEE, SANG-HYUN
10278991	6692112	150	10/24/2002	MONOLITHIC INK-JET PRINTHEAD	LEE, SANG-HYUN
09943029	Not Issued	071	08/29/2001	DATA RECOVERY USING DATA EYE TRACKING	LEE, SANG-HYUN
09376762	6215149	150	08/17/1999	SEMICONDUCTOR DEVICE HAVING A TRENCH TYPE GATE AND A FABRICATION METHOD THEREFOR	LEE, SANG-HYUN
09332732	Not Issued	160	06/14/1999	POWER DEVICE AND METHOD OF MANUFACTURING THE SAME	LEE, SANG-HYUN
09299739	6473664	150	04/27/1999	MANUFACTURING PROCESS AUTOMATION SYSTEM USING A FILE SERVER AND ITS CONTROL METHOD	LEE, SANG-HYUN
08956105	5940336	150	10/24/1997	REFERENCE CLOCK GENERATING CIRCUIT IN MEMORY TO BE ASYNCHRONOUSLY PRECHARGED AND ACTIVATED	LEE, SANG-HYUN
08903876	5825693	150	07/31/1997	WRITE CONTROL CIRCUIT FOR SEMICONDUCTOR MEMORY	LEE, SANG-HYUN

08901627	5883846	150	07/28/1997	LATCH TYPE SENSE AMPLIFIER HAVING A NEGATIVE FEEDBACK DEVICE	LEE, SANG-HYUN
07806938	D346161	150	12/11/1991	KEYBOARD FOR A COMPUTER	LEE, SANG-HYUN
07806923	D346588	150	12/11/1991	COMPUTER	LEE, SANG-HYUN
07806922	D346371	150	12/11/1991	DISPLAY FOR COMPUTER	LEE, SANG-HYUN

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Last Name = JEONG
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Application#	Patent#	Status	Date Filed	Title	Inventor Name 50
60378572	Not Issued	159	05/06/2002	IP ADDRESS LOOKUP SCHEME	JEONG, DEOG-KYOON
60378524	Not Issued	159	05/06/2002	PRIORITY QUEUE FOR HIGH-SPEED PACKET SWITCHES	JEONG, DEOG-KYOON
60378523	Not Issued	159	05/06/2002	SCHEDULER FOR MULTIPLANE CROSSBAR SWITCHES	JEONG, DEOG-KYOON
60230589	Not Issued	159	09/05/2000	OVERSAMPLING TRANSCEIVER WITH DEAD-ZONE PHASE DETECTION	JEONG, DEOG-KYOON
60229369	Not Issued	159	08/30/2000	DATA RECOVERY USING DATA EYE TRACKING	JEONG, DEOG-KYOON
60187370	Not Issued	159	03/06/2000	METHOD AND APPARATUS FOR SERIAL INTERFACE FOR STORAGE DEVICE	JEONG, DEOG-KYOON
60176416	Not Issued	159	01/14/2000	BAUD-RATE TIMING RECOVERY	JEONG, DEOG-KYOON
60164874	Not Issued	159	11/12/1999	RECEIVER	JEONG, DEOG-KYOON
60136640	Not Issued	159	05/27/1999	UNLIMITED FREQUENCY RANGE DELAY-LOCKED LOOP CIRCUIT	JEONG, DEOG-KYOON
60071879	Not Issued	159	01/20/1998	1.25GBAUD CMOS DRIVER AND ON-CHIP TERMINATION FOR GIGABIT ETHERNET PHY CHIP	JEONG, DEOG-KYOON
60071805	Not Issued	159	01/20/1998	SUPPRESSION OF ELECTROMAGNETIC INTERFERENCE IN PARALLEL DATA CHANNELS THROUGH SPREAD SPECTRUM PHASE MODULATION	JEONG, DEOG-KYOON
60058042	Not Issued	159	09/04/1997	POWER SAVING METHODS FOR COLUMN DRIVERS	JEONG, DEOG-KYOON
60058041	Not Issued	159	09/04/1997	DATA DRIVING WITH REDUCED EMI	JEONG, DEOG-KYOON
60058040	Not Issued	159	09/04/1997	DATA RECOVERY SCHEME FOR OVERSAMPLED SYSTEMS	JEONG, DEOG-KYOON
11056995	Not	019	02/11/2005	PHASE LOCK LOOP WITH COARSE	JEONG, DEOG-

	Issued			CONTROL LOOP HAVING FREQUENCY LOCK DETECTOR AND DEVICE INCLUDING SAME	KYOON
10652721	Not Issued	160	08/29/2003	CMOS TRANSCEIVER WITH DUAL CURRENT PATH VCO	JEONG, DEOG-KYOON
10651500	Not Issued	030	08/29/2003	CMOS TRANSCEIVER WITH DUAL CURRENT PATH VCO	JEONG, DEOG-KYOON
10642259	Not Issued	030	08/15/2003	DATA SAMPLING METHOD AND APPARATUS WITH ALTERNATING EDGE SAMPLING PHASE DETECTION FOR LOOP CHARACTERISTIC STABILIZATION	JEONG, DEOG-KYOON
10613442	6888417	150	07/03/2003	VOLTAGE CONTROLLED OSCILLATOR	JEONG, DEOG-KYOON
10612840	Not Issued	030	07/03/2003	TRACKED 3X OVERSAMPLING RECEIVER	JEONG, DEOG-KYOON
10403477	6819166	150	03/31/2003	CONTINUOUS-TIME, LOW-FREQUENCY-GAIN/HIGH-FREQUENCY-BOOSTING JOINT ADAPTATION EQUALIZER AND METHOD	JEONG, DEOG-KYOON
10113600	6538498	150	04/02/2002	GM-C TUNING CIRCUIT WITH FILTER CONFIGURATION	JEONG, DEOG-KYOON
10053461	Not Issued	041	11/07/2001	METHOD AND SYSTEM FOR COMMUNICATING CONTROL INFORMATION VIA OUT-OF-BAND SYMBOLS	JEONG, DEOG-KYOON
10045625	Not Issued	030	11/07/2001	METHOD AND SYSTEM FOR INTEGRATING PACKET TYPE INFORMATION WITH SYNCHRONIZATION SYMBOLS	JEONG, DEOG-KYOON
10045606	Not Issued	030	11/07/2001	METHOD AND SYSTEM FOR DYNAMIC SEGMENTATION OF COMMUNICATIONS PACKETS	JEONG, DEOG-KYOON
10045601	Not Issued	061	11/07/2001	MULTISECTION MEMORY BANK SYSTEM	JEONG, DEOG-KYOON
10045393	Not Issued	030	11/07/2001	METHOD AND SYSTEM FOR TRANSITION-CONTROLLED SELECTIVE BLOCK INVERSION COMMUNICATIONS	JEONG, DEOG-KYOON
10045348	Not Issued	030	11/07/2001	METHOD AND SYSTEM FOR ASYMMETRIC PACKET ORDERING BETWEEN COMMUNICATIONS DEVICES	JEONG, DEOG-KYOON
10045297	Not Issued	061	11/07/2001	COMMUNICATIONS ARCHITECTURE FOR MEMORY-BASED DEVICES	JEONG, DEOG-KYOON

10035911	Not Issued	030	11/07/2001	METHOD AND SYSTEM FOR NESTING OF COMMUNICATIONS PACKETS	JEONG, DEOG-KYOON
09766503	Not Issued	160	01/18/2001	HIGH SPEED SERIAL LINK FOR FULLY DUPLEXED DATA COMMUNICATION	JEONG, DEOG-KYOON
09759624	6891910	150	01/12/2001	BAUD-RATE TIMING RECOVERY	JEONG, DEOG-KYOON
09709637	6483355	150	11/13/2000	SINGLE CHIP CMOS TRANSMITTER/RECEIVER AND METHOD OF USING SAME	JEONG, DEOG-KYOON
09574571	6326826	150	05/17/2000	WIDE FREQUENCY-RANGE DELAY-LOCKED LOOP CIRCUIT	JEONG, DEOG-KYOON
09393849	6738417	150	09/09/1999	METHOD AND APPARATUS FOR BIDIRECTIONAL DATA TRANSFER BETWEEN A DIGITAL DISPLAY AND A COMPUTER	JEONG, DEOG-KYOON
09298369	6374361	150	04/22/1999	SKEW-INSENSITIVE LOW VOLTAGE DIFFERENTIAL RECEIVER	JEONG, DEOG-KYOON
09234619	6560290	150	01/20/1999	CMOS DRIVER AND ON-CHIP TERMINATION FOR GIGABAUD SPEED DATA COMMUNICATION	JEONG, DEOG-KYOON
09007707	5969552	150	01/15/1998	DUAL LOOP DELAY-LOCKED LOOP	JEONG, DEOG-KYOON
08815486	6157360	150	03/11/1997	SYSTEM AND METHOD FOR DRIVING COLUMNS OF AN ACTIVE MATRIX DISPLAY	JEONG, DEOG-KYOON
08664136	5835498	150	06/14/1996	SYSTEM AND METHOD FOR SENDING MULTIPLE DATA SIGNALS OVER A SERIAL LINK	JEONG, DEOG-KYOON
08631420	5815041	150	04/12/1996	HIGH-SPEED AND HIGH-PRECISION PHASE LOCKED LOOP HAVING PHASE DETECTOR WITH DYNAMIC LOGIC STRUCTURE	JEONG, DEOG-KYOON
08581135	5802103	150	12/29/1995	HIGH SPEED SERIAL LINK FOR FULLY DUPLEXED DATA COMMUNICATION	JEONG, DEOG-KYOON
08580914	5712585	150	12/29/1995	A SYSTEM FOR DISTRIBRITING CLOCK SIGNALS	JEONG, DEOG-KYOON
08580700	5675584	150	12/29/1995	HIGH SPEED SERIAL LINK FOR FULLY DUPLEXED DATA COMMUNICATION	JEONG, DEOG-KYOON
08580571	5587709	150	12/29/1995	HIGH SPEED SERIAL LINK FOR FULLY DUPLEXED DATA COMMUNICATION	JEONG, DEOG-KYOON
08580569	5705947	150	12/29/1995	CLOCK GENERATOR	JEONG, DEOG-KYOON

08415056	5712884	150	03/31/1995	DATA RECEIVING METHOD AND CIRCUIT OF DIGITAL COMMUNICATION SYSTEM	JEONG, DEOG-KYOON
08370904	5621407	150	01/10/1995	DIGITAL/ANALOG CONVERTER	JEONG, DEOG-KYOON
08332561	5574756	150	10/31/1994	METHOD FOR GENERATING DIGITAL COMMUNICATION SYSTEM CLOCK SIGNALS & CIRCUITRY FOR PERFORMING THAT METHOD	JEONG, DEOG-KYOON
08254326	5714904	150	06/06/1994	HIGH SPEED SERIAL LINK FOR FULLY DUPLEXED DATA COMMUNICATION	JEONG, DEOG-KYOON

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Application#	Patent#	Status	Date Filed	Title	Inventor Name 39
60437856	Not Issued	159	01/03/2003	CMOS 3.5 GBPS CONTINUOUS-TIME, LOW-FREQUENCY-GAIN/HIGH-FREQUENCY-BOOSTING JOINT ADAPTATION EQUALIZER AND METHOD	JEONG, DEOG-KYOON
60416017	Not Issued	159	10/04/2002	2.5-10GBPS CMOS TRANSCEIVER WITH ALTERNATING EDGE SAMPLING PHASE DETECTION FOR LOOP CHARACTERISTIC STABILIZATION	JEONG, DEOG-KYOON
60406858	Not Issued	159	08/29/2002	CMOS TRANSCEIVER WITH DUAL CURRENT PATH VCO	JEONG, DEOG-KYOON
60333439	Not Issued	159	11/26/2001	0.6-2.5GBAUD CMOS TRACKED 3X OVERSAMPLING TRANSCEIVER WITH DEAD-ZONE PHASE DETECTION FOR ROBUST CLOCK/DATA RECOVERY	JEONG, DEOG-KYOON
60296652	Not Issued	159	06/06/2001	DATA ENCODING BASED ON TRANSITION-CONTROLLED SELECTIVE BLOCK INVERSION	JEONG, DEOG-KYOON
60296213	Not Issued	159	06/05/2001	SCALABLE STORAGE INTERFACE ARCHITECTURE	JEONG, DEOG-KYOON
60252724	Not Issued	159	11/22/2000	METHOD AND APPARATUS FOR STORAGE I/O WITH FULL-DUPLEX ONE-TIME BLOCK I/O TRANSFER AND ADAPTIVE PAYLOAD SIZING	JEONG, DEOG-KYOON
60100057	Not Issued	159	09/10/1998	METHODS AND APPARATUS FOR BIDIRECTIONAL DATA TRANSFER BETWEEN DIGITAL DISPLAY DEVICE AND COMPUTING DEVICES	JEONG, DEOG-KYOON
60082959	Not Issued	159	04/23/1998	SKEW-INSENSITIVE LVDS (LOW VOLTAGE DIFFERENTIAL SWING) RECEIVER	JEONG, DEOG-KYOON
10722842	6876240	150	11/25/2003	WIDE RANGE MULTI-PHASE DELAY-LOCKED LOOP	JEONG, DEOG-KYOON

10356695	6859107	150	01/30/2003	FREQUENCY COMPARATOR WITH HYSTERESIS BETWEEN LOCKED AND UNLOCKED CONDITIONS	JEONG, DEOG-KYOON
10305254	Not Issued	030	11/25/2002	0.6-2.5 GBAUD CMOS TRACKED 3X OVERSAMPLING TRANSCEIVER WITH DEAD ZONE PHASE DETECTION FOR ROBUST CLOCK/DATA RECOVERY	JEONG, DEOG-KYOON
10253534	6781424	150	09/25/2002	SINGLE CHIP CMOS TRANSMITTER/RECEIVER AND METHOD OF USING SAME	JEONG, DEOG-KYOON
10215936	6717468	150	08/08/2002	DYNAMICALLY BIASED FULL-SWING OPERATION AMPLIFIER FOR AN ACTIVE MATRIX LIQUID CRYSTAL DISPLAY DRIVER	JEONG, DEOG-KYOON
10196479	6756828	150	07/17/2002	PHASE LOCK LOOP (PLL) APPARATUS AND METHOD	JEONG, DEOG-KYOON
10183974	Not Issued	094	06/25/2002	HIGH-SPEED AND HIGH-PRECISION PHASE LOCKED LOOP	JEONG, DEOG-KYOON
10045600	6771192	150	11/07/2001	METHOD AND SYSTEM FOR DC-BALANCING AT THE PHYSICAL LAYER	JEONG, DEOG-KYOON
10037168	Not Issued	030	11/07/2001	METHOD AND SYSTEM FOR PLESIOSYNCHRONOUS COMMUNICATIONS WITH NULL INSERTION AND REMOVAL	JEONG, DEOG-KYOON
10036794	Not Issued	090	11/07/2001	METHOD AND SYSTEM FOR HOST HANDLING OF COMMUNICATIONS ERRORS	JEONG, DEOG-KYOON
10036135	Not Issued	030	11/07/2001	METHOD AND SYSTEM FOR PACKET ORDERING BASED ON PACKET TYPE	JEONG, DEOG-KYOON
10035591	Not Issued	030	11/07/2001	COMMUNICATIONS ARCHITECTURE FOR STORAGE-BASED DEVICES	JEONG, DEOG-KYOON
09985897	6512408	150	11/06/2001	MIXER STRUCTURE AND METHOD FOR USING SAME	JEONG, DEOG-KYOON
09948123	Not Issued	164	09/05/2001	IMPLEMENTING AN OVERSAMPLING TRANSCEIVER WITH DEAD-ZONE PHASE DETECTION	JEONG, DEOG-KYOON
09943029	Not Issued	071	08/29/2001	DATA RECOVERY USING DATA EYE TRACKING	JEONG, DEOG-KYOON
09897975	6510185	150	07/05/2001	SINGLE CHIP CMOS TRANSMITTER/RECEIVER	JEONG, DEOG-KYOON
09814256	6587525	150	03/21/2001	SYSTEM AND METHOD FOR HIGH-SPEED, SYNCHRONIZED DATA COMMUNICATION	JEONG, DEOG-KYOON

09693516	6462624	150	10/20/2000	HIGH-SPEED AND HIGH-PRECISION PHASE LOCKED LOOP	JEONG, DEOG-KYOON
09234777	6600771	150	01/20/1999	SPREAD SPECTRUM PHASE MODULATION FOR SUPPRESSION OF ELECTROMAGNETIC INTERFERENCE IN PARALLEL DATA CHANNELS	JEONG, DEOG-KYOON
09187559	6151334	150	11/04/1998	SYSTEM AND METHOD FOR SENDING MULTIPLE DATA SIGNALS OVER A SERIAL LINK	JEONG, DEOG-KYOON
09148815	6144242	150	09/04/1998	CONTROLLABLE DELAYS IN MULTIPLE SYNCHRONIZED SIGNALS FOR REDUCED ELECTROMAGNETIC INTERFERENCE AT PEAK FREQUENCIES	JEONG, DEOG-KYOON
09148583	6271816	150	09/04/1998	POWER SAVING CIRCUIT AND METHOD FOR DRIVING AN ACTIVE MATRIX DISPLAY	JEONG, DEOG-KYOON
09146818	6229859	150	09/04/1998	SYSTEM AND METHOD FOR HIGH-SPEED, SYNCHRONIZED DATA COMMUNICATION	JEONG, DEOG-KYOON
09098266	6157263	150	06/16/1998	HIGH-SPEED AND HIGH-PRECISION PHASE LOCKED LOOP HAVING PHASE DETECTOR WITH DYNAMIC LOGIC STRUCTURE	JEONG, DEOG-KYOON
09017758	6107946	150	02/03/1998	HIGH SPEED SERIAL LINK FOR FULLY DUPLEXED DATA COMMUNICATION	JEONG, DEOG-KYOON
09013679	6211714	150	01/26/1998	PARALLEL CONDUCTOR SYSTEM FOR REDUCING NOISE IN TRANSMITTING CLOCK SIGNALS	JEONG, DEOG-KYOON
08937262	6100868	150	09/15/1997	HIGH DENSITY COLUMN DRIVERS FOR AN ACTIVE MATRIX DISPLAY	JEONG, DEOG-KYOON
08920336	5955929	150	08/27/1997	VOLTAGE-CONTROLLED OSCILLATOR RESISTANT TO SUPPLY VOLTAGE NOISE	JEONG, DEOG-KYOON
08000430	5332934	150	01/04/1993	SMALL TO FULL SWING CONVERSION CIRCUIT	JEONG, DEOG-KYOON

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